Marinchip Systems M9900 PROM/RAM/SIO/RTC
Theory of Operation and Configuration Guide

by John Walker

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Marinchip Systems

computer hardware and software

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1. Introduction

The Marinchip 9900 PROM/RAM/SIO/RTC board is designed to be used with the Marinchip Systems M9900 CPU. It combines on a single board the functions of a PROM board, scratchpad RAM, Serial I/O board, and real-time clock. The unique CRU I/O architecture of the TMS9900 allows all of these functions to be combined on a single board without the need for an expensively dense board layout.

The PROM/RAM section of the board operates in 16 bit moce with the M9900 CPU. Hence, all memory accesses serviced from this board will execute three times faster than those referencing 8 bit S-100 memory. This will yield a two-to-one increase in actual execution speed for programs executing out of the memory on the PROM/RAM board.

This manual will first explain the jumper-selectable options on the board. Properly jumpering these options is required for correct operation of the board. A subsequent chapter explains the internal operation of the board.

1.1. Normal board configuration

The PROM/RAM board is normally used in the M9900 system to hold the debug monitor / disc boot PROM, to provide the scratchpad RAM and workspace register storage, and to provide the serial I/O port that interfaces the system console. The portions of the system address space used by the board in this normal configuration are:

```
Scratchpad RAM:  F400-F7FF
Boot PROM:       F800-FFFF
Serial I/O, RTC:  000- 01F   (CRU address)
```

The two user PROM sockets can hold 2K, 4K, or 8K of PROM, and can be placed starting at any 2K, 4K, or 8K boundary, respectively, in memory. When these sockets are not being used, they are disabled and occupy no address space.

2. Option jumper selections

The M9900 PROM/RAM board contains 6 option jumper sockets. Options are selected by soldering jumper wires across DIP header plugs between the pins indicated in the text below. The DIP header plug is then inserted in the specified option socket. When you hold the board with component side up and the long edge connector toward you, all the option jumper sockets will be horizontal. Pin 1 is the pin in the lower left corner.

2.1. Serial I/O, Real time clock jumpers

The following jumper selections set the CRU starting address of the TMS9902 chip and the interrupt level used for the I/O and clock.

2.1.1. CRU address selection

The CRU base address of the serial I/O port and real time clock are set by the jumpers in option sockets S26 (position 9J) and S35 (position 8K). To use the board in a standard M9900 system, the base address should be set to zero. To jumper for the standard address, connect the following pins:

In S26: 1-16
In S35: 1-16 5-12

The following information describes how to jumper the port for any CRU address. If the port is set to a nonzero address, the serial I/O port will not work with standard Marinchip software releases, so the port should be set to another address only in custom systems, or when using the PROM/RAM board as an I/O board only.

The CRU address space consists of 4096 individually addressable bits. This space is addressed by 12 address bits. The TMS9902 SIO/RTC chip occupies 32 bits of this address space, and hence uses the low-order 5 address bits as an internal bit address. Consequently, the user must select the value of the top 7 address bits to select the CRU address of the port. To do this, select the CRU address desired for the port. This address is normally specified as a three digit hexadecimal number. As an example, we will choose C80.

Write the hexadecimal address as a binary number, e.g.,

1100 1000 0000

Cross off the low five bits, as they are irrelevant to the board jumpering:

1100 100- ----

Look at the leftmost two bits in the number, and install a jumper in socket S35 based on the value of the bits, referring to the following table:

Bits Jumper Position

00	S35:	1-16
01	S35:	2-15
10	S35:	3-14
11	S35:	4-13

For our example, we would have installed a jumper from pin 4 to pin 13 in S35 because the leftmost two bits were 11. Now cross off the leftmost two bits. In our example, this would leave:

--00 100- ----

Now look at the next two bits (after the leftmost two have been crossed off. Referring to the following table, install a second jumper in socket S35 based on the value of the bits.

Bits	Jumper Position	
00	S35:	5-12
01	S35:	6-11
10	S35:	7-10
11	S35:	8-9

For our example, we would have installed the jumper from pin 5 to pin 12 in S35, because the two bits were 00. Cross off the two bits just selected. In our example, we would then have:

---- 100- ----

Finally, install a single jumper in socket S26 (position 9J) based on the value of the three remaining bits. Refer to the following table for the jumper position:

Bits	Jumper Position	
000	S26:	1-16
001	S26:	2-15
010	S26:	3-14
011	S26:	4-13
100	S26:	5-12
101	S26:	6-11
110	S26:	7-10
111	S26:	8-9

In our example, we would jumper pin 5 to pin 12 in S26 because the remaining 3 bits of the address were 100. This completes the jumpering of the serial I/O and real time clock address.

2.1.2. Interrupt level selection

The Serial I/O port and real time clock are capable of generating interrupts when certain events transpire. A jumper installed in option socket S10 (at position 1E) selects whether this interrupt will be generated, and at what level the interrupt request will be made.

The Marinchip Disc Executive does not use interrupts from the serial I/O port or real time clock, so for this system the jumper should not be installed in the socket.

The Marinchip Network Operating system requires that the SIO/RTC interrupt be jumpered to interrupt level 2. For this system, the jumper should be installed between pins 3 and 14 in S10.

The user may jumper the SIO/RTC interrupt to any desired level by referring to the table below:

Level	Jumper Position	
0	S10: 1-16	(Warning: causes RESET!)
1	S10: 2-15	
2	S10: 3-14	
3	S10: 4-13	
4	S10: 5-12	
5	S10: 6-11	
6	S10: 7-10	
7	S10: 8-9	

2.1.3. Serial I/O type selection

The serial I/O port generates control signals which permit it to be connected either to a terminal device, or to a modem to allow dial-up access to the system. The terminal and modem controls are generated simultaneously by the board and presented on the two 26 pin edge connectors at the top of the board. If the SIO port is to be connected to a TERMINAL, plug the connector onto connector J2 (the LEFT connector). If the SIO port is to be connected to a MODEM, plug the connector onto connector J1 (the RIGHT connector).

2.2. Utility PROM option selection

The two 24 pin sockets, U47 (position 9N) and U57 (position 9S) may be used for user PROM storage. When the board is supplied, these sockets are not populated with PROMs, and the PROM storage is disabled by the absence of PROM address selection jumpers. These sockets may be filled with a number of different types of PROMs, yielding different amounts of total PROM storage. All the PROMs used are organised such that 8 bits of data are output by the PROM for each address read. The two PROMs supply the 16 bit word transferred to the processor when a read request occurs. When installing the PROMs in the sockets, the PROM with the even bytes (most significant byte) should be placed in socket U47 (left socket), and the PROM with the odd bytes (least significant byte) should be placed in socket U57 (right socket).

The jumpering options below are given for each type of PROM that can be used in the sockets. The option jumpers referred to are installed in sockets S36 (position 9L), S33 (position 4K), and S23 (position 5H). The jumpering of socket S36 selects the power and addressing configuration of the PROM. If incorrectly jumpered, THE PROMs MAY BE DESTROYED. Check the jumpering of S36 against the instructions below at least three times before installing the board in your computer and applying power.

2.2.1. 2708 PROM (2K total storage)

The 2708 PROM is a 1K X 8 PROM. Use of this part results in a total capacity of 2K for the user PROM sockets. The socket at S36 must be

strapped as follows:

2708 S36 Strapping

S36: 5-10
S36: 6-9
S36: 2-13

The two 2708 PROMs will fill a 2K byte portion of the address space. This area may be placed at any 2K boundary in memory by selection of options in sockets S23 (position 5H) and S33 (position 4K). To determine the required options, write the address desired for the first byte of the 2K area. Strap S33 based on the three most significant bits of the address according to the following table:

Bits	S33 Strapping
000	1-16
001	2-15
010	3-14
011	4-13
100	5-12
101	6-11
110	7-10
111	8-9

S23 should then be jumpered based upon the next two bits in the PROM area starting address according to the following table:

Bits	S23 Strapping
00	4-11
01	3-12
10	2-13
11	1-14

For example, suppose we want the 2K PROM page to start at address B800. Expressed in binary, this is 1101 1000 0000 0000. The top three bits of this value are 110. From the first table above, we can see that S33 should be strapped 7-10. The next two bits are 11, so from the second table we can see that S23 should be strapped 1-14.

The same strapping is used for the 2308 ROM.

2.2.2. 2516 PROM (4K total storage)

The 2516 PROM is a 2K X 8 PROM. The number 2516 is Texas Instruments' number for this part; Intel designates this part as 2716. Unfortunately, there is a TMS2716 made by Texas Instruments, which is NOT THE SAME. The TMS2716 will not run in the M9900 PROM/RAM board (without cutting traces), so make sure you use an Intel 2716, or a T.I. 2516 PROM with the following instructions.

2516 S36 Strapping

S36: 5-10
S36: 7-8

S36: 1-14

The two 2516 PROMs will fill a 4K byte portion of the address space. This area may be placed at any 4K boundary in memory by selection of options in sockets S23 (position 5H) and S33 (position 4K). To determine the required options, write the address desired for the first byte of the 4K area. Strap S33 based on the three most significant bits of the address according to the following table:

Bits	S33 Strapping
000	1-16
001	2-15
010	3-14
011	4-13
100	5-12
101	6-11
110	7-10
111	8-9

S23 should then be jumpered based upon the next bit in the PROM area starting address according to the following table:

Bit	S23 Strapping
0	5-10
1	6-9

For example, suppose we want the 4K PROM page to start at address B000. Expressed in binary, this is 1101 0000 0000 0000. The top three bits of this value are 110. From the first table above, we can see that S33 should be strapped 7-10. The next bit is 1, so from the second table we can see that S23 should be strapped 6-9.

The same strapping is used for the 2316E ROM.

2.2.3. 2532 PROM (8K total storage)

The 2532 PROM is a 4K X 8 PROM. The S36 options should be set as follows:

2532 S36 Strapping

S36: 5-10
S36: 7-8
S36: 3-12

The two 2532 PROMs will fill a 8K byte portion of the address space. This area may be placed at any 8K boundary in memory by selection of options in sockets S23 (position 5H) and S33 (position 4K). To determine the required options, write the address desired for the first byte of the 8K area. Strap S33 based on the three most significant bits of the address according to the following table:

Bits	S33 Strapping
000	1-16

001	2-15
010	3-14
011	4-13
100	5-12
101	6-11
110	7-10
111	8-9

S23 should be jumpered 7-8.

For example, suppose we want the 8K PROM page to start at address C000. Expressed in binary, this is 1100 0000 0000 0000. The top three bits of this value are 110. From the first table above, we can see that S33 should be strapped 7-10. S23 should be strapped 7-8, as it always is when using 2532 PROMs.

3. Theory of operation

This section describes the internal operation of the PROM/RAM/SIO/RTC board. Signal named used in this discussion will correspond to the names used in the logic drawings, except that a signal which is low when asserted will be indicated by a trailing hyphen (e.g., EXPLODE-) rather than an overbar.

The board is divided into two distinct subsystems: the PROM/RAM memory area, and the SIO/RTC logic. These sections share only the address decoder.

3.1. PROM/RAM section

The PROM/RAM section consists of the PROM and RAM memory arrays, the data bus buffer, and the addressing and control logic. The memory array and bus buffer sections consist of two identical 8 bit wide subsections, always used in parallel for a 16 bit memory transfer. All the chips used in the most significant byte of a word (even address) are numbered U4x, and all chips used in the least significant byte (odd address) are numbered U5x. For example, U43 is a 2111 RAM used in the most significant byte of the RAM area. U53 is the corresponding RAM used in the least significant byte.

3.1.1. Memory array

The 2K boot PROM, provided by 2 2708 PROMs at U46 and U56, the 1K scratchpad RAM provided by the 8 2111's U42-U45 and U52-U55, and the 2K/4K/8K user PROM provided by the two optional PROMs at U47 and U57 are all or-tied together. Only the memory circuit actually selected for reading drives the data lines, and that data is copied to the S-100 data lines by the 8304 buffer circuits U41 and U51. During write operations, the 8304s copy the data from the bus so that the RAMs can be properly written.

The 2708 is a 1K X 8 PROM. It is driven with the low-order 10 address bits A10 through A1 (A0 designates the addressed byte of S-100 memory and is ignored in sixteen bit mode). Its output is enabled to the common data bus only when the address bus is between F800 and FFFF (see addressing logic explanation below).

The 2111 is a 256 X 4 RAM. The 2111's are arranged into two banks of four RAMs each. Each bank provides 256 X 16 (or 1/2 K bytes) of storage. With both banks populated, a total of 1K of RAM is provided. The 2111's are supplied with two chip enable signals, one which is activated when any 2111 is addressed, and the other which selects the specific bank. The output enable and write control signals for the RAMs are derived from the S-100 control signals.

The user PROM area can accomodate 2708, 2516, or 2532 PROMs. Each of these PROMs contain 1K, 2K, or 4K X 8 bits respectively. Except that no two memory boards in a system may have the same addresses, the PROMs can be placed at any address in memory on a boundary equal to their memory capacity (2K for 2708, 4K for 2516, and 8K for 2532). The address decoding for the PROMs is done by jumper-selecting the output of decoders (see addressing logic below). Since the PROMs have

different supply voltages and address bit configurations, socket S36 permits selection of the signals that drive pins 18, 19, and 21 of the PROMs. The following table describes the signal selections for each strapping option.

Pin	Signal	S36 Strap
18	OE-	4-11
18	GND	5-10
19	+12	6-9
19	A11	7-8
21	+5	1-14
21	-5	2-13
21	A12	3-12

Note that only one signal may be selected to drive a pin of the PROM. Refer to chapter 2 of this manual for information on the recommended strapping for various PROMs.

3.1.2. Bus buffer

The 16 bit bidirectional data bus, consisting of the S-100 data out lines (for the bytes at even addresses) and the S-100 data in lines (for the odd bytes), is buffered and driven by the two 8304 bidirectional bus driver/receiver chips at U41 and U51. The 8304 buffers are enabled by DEBL-, which is generated by the addressing/control logic whenever the memory section of the board is addressed. The buffers copy data from the memory circuits' data bus onto the S-100 bus unless the signal RAMWE- is true. If this signal is true, the cycle is writing into the RAM, so data will be driven onto the internal data bus from the S-100 data lines.

3.1.3. Addressing and control logic

The three most significant S-100 address lines (A15, A14, and A13) are decoded by U32, a 74LS138 three to eight demultiplexor. This demultiplexor is activated only when the M9900 IO signal (S-100 pin 96) is low, so selection will occur only on memory cycles. The output of this decoder generates the signal MSB111- when the top three address bits are 111, and MSBXXX- when the top three bits equal the value strapped in option socket S33. (MSBXXX- is the select signal used in addressing the user PROM).

Address bits A12 through A1 are buffered by 74LS241 octal bus buffers U21 and U31. A12, A11, A10, and A9 are decoded by U34, a 74LS139 dual two to four demultiplexor. If A12 and A11 decode to 11, the signal 2708SEL- is asserted, which in combination with MSB111- and PDBIN enables the 2708 boot PROMs for addresses between F800 and FFFF.

If A12 and A11 decode to 10, the signal 1211B10- is asserted. This signal, in combination with MSB111- generates RAMSEL1-, which is a general chip enable sent to all the 2111 RAMs. If A10 and A9 decode to 10, the signal RAMSEL2A- is asserted, which serves as the specific chip enable for the lower bank of 2111 RAMs (U42, U44, U52, U54). If A10 and A9 decode to 11, the signal RAMSEL2B- is asserted. This

serves as the specific chip enable for the upper bank of 2111 RAMs (U43, U45, U53, U55). Since the 2111 is selected only if both chip enables are true, this will serve to enable the lower 2111's for the address range F400-F5FF and the upper 2111's for the range F600-F7FF.

If the user PROMs are installed, their start address is selected by jumpering the 8K region of memory in which they reside via an option strap in S33. Selection of a 2K, 4K, or the entire 8K area is accomplished by installing a jumper in S23. The following table describes the proper jumpers for user PROM.

8K Area	S33 Strap
0000-1FFF	1-16
2000-3FFF	2-15
4000-5FFF	3-14
6000-7FFF	4-13
8000-9FFF	5-12
A000-BFFF	6-11
C000-DFFF	7-10
E000-FFFF	8-9

Region	Size	S23 Strap
0000-07FF	2K	4-11
0800-0FFF	2K	3-12
1000-07FF	2K	2-13
1800-1FFF	2K	1-14
0000-0FFF	4K	5-10
1000-1FFF	4K	6-9
0000-1FFF	8K	7-8

Only one jumper should be installed in S23, and one jumper should be installed in S33.

Whenever a memory cycle is being serviced by the board, the S-100 line SXTN- is pulled to ground. This will cause the M9900 CPU to perform a parallel 16 bit transfer insteac of the normal pair of 8 bit transfers.

3.2. Serial I/O, Real time clock section

The serial I/O port and real time clock functions of the board are provided by the TMS9902 Asynchronous Communication Controller chip. The user is referred to the Texas Instruments data manual describing this chip for its internal operation. The TMS9902 is a CRU peripheral, and is connected to the CRU and address bus lines of the M9900 CPU. The SIO/RTC section of the board is divided into three sections: CRU buffering, Addressing and selection logic, and RS-232 drivers and receivers.

3.2.1. CRU buffers

The PCRUOUT(13) and PCRUCLK-(12) S-100 lines are buffered by 74LS241 buffer U21. PCRUCLK- is inverted, and the buffered signals are

presented to the TMS9902 as CRUOUT and CRUCLK. When the TMS9902 is addressed, the 74LS125 tristate bus driver U11 will drive the CRUIN pin from the TMS9902 onto the S-100 PCRUIN(14) line. The system master clock TWOMHZ(49) is buffered by U21, and provides the baud rate and real time clock input to the TMS9902.

3.2.2. Addressing and selection

The TMS9902 chip enable signal is activated when the 32 bit area of CRU address space containing the chip is addressed. The CRU address of the chip is strapped by jumpers in the option sockets S35 (which select the top 4 bits of the address) and S26 (which select the next 3 bits of the address). Detailed strapping instructions are given in chapter 2 of this manual; refer to them for detailed information on jumpering the CRU address. The decoding of the top 4 bits of CRU address uses the 74LS139 decoder U34 which is also used by the PROM/RAM section. The 74LS138 decoder U25, which decodes the next three bits of CRU address, is dedicated to the SIO/RTC section.

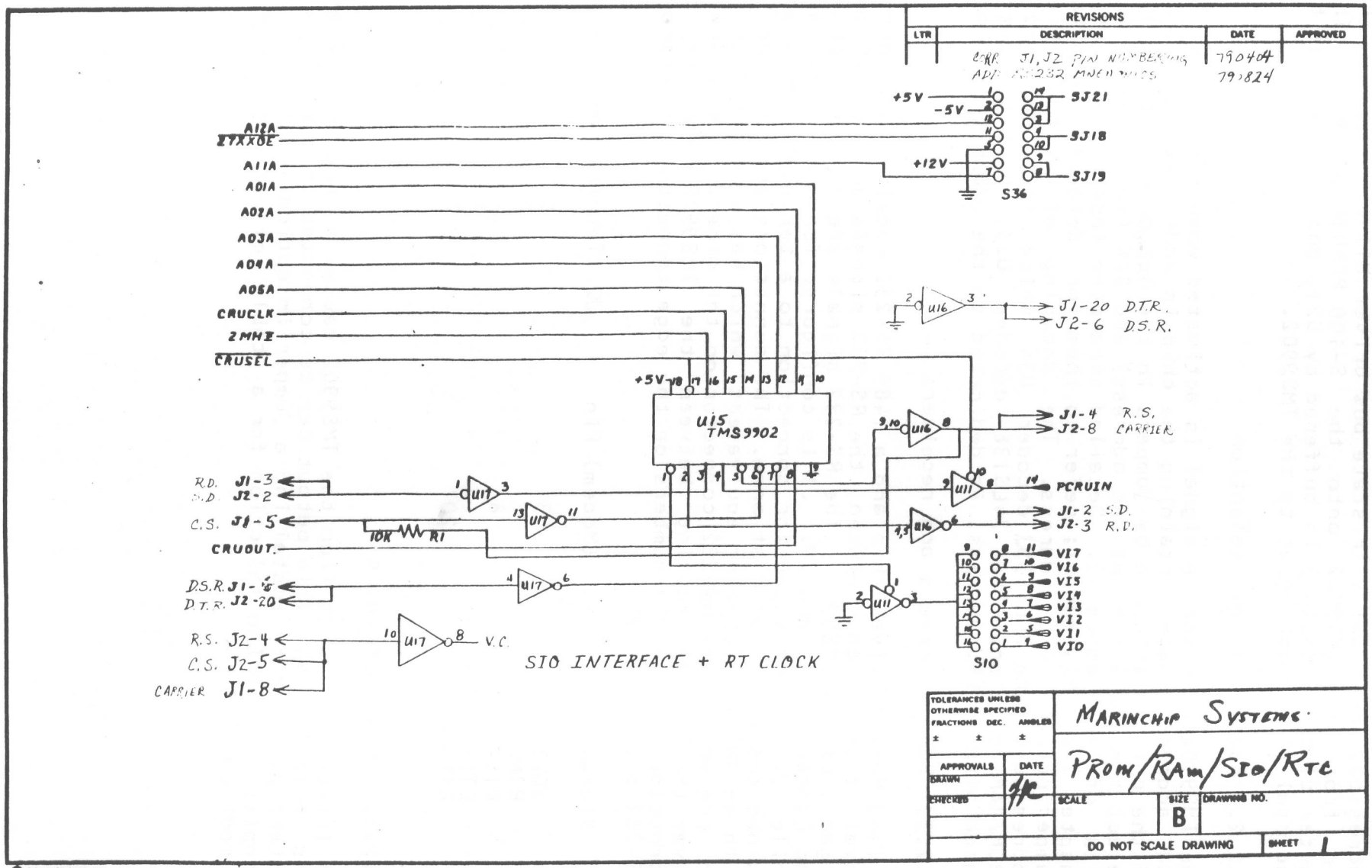
3.2.3. RS-232 drivers and receivers

A 1488 RS-232 driver chip and a 1489 RS-232 receiver chip perform the level translation between the RS-232 signals and the TTL-compatible signals of the TMS9902. The RS-232 signals are presented on the two top connectors J1 and J2. J1 is configured for connection to a modem, while J2 is connected for connection to a terminal. Only one of the connectors may be used at once. The connectors are designed to mate with an IMSAI CABLE-A or equivalent, which has a 26 pin edge connector on one end and an RS-232 connector on the other. The following table gives the signal routing between the TMS9902 and the two edge connectors. (The pin numbers on the edge connectors correspond to the RS-232 pin numbers).

Signal name	J1 (Modem) Pin	J2 (Terminal pin)
XOUT	3	2
RIN	2	3
RTS-	8	4
CTS-		5
DSR-	20	8

3.2.4. Interrupt logic

An interrupt request from the TMS9902 causes a tristate driver to pull its output low. This output can be connected to any of the vectored interrupt lines by installing a jumper in option socket S10. Refer to chapter 2 on option selection for a table of interrupt levels and jumper positions.



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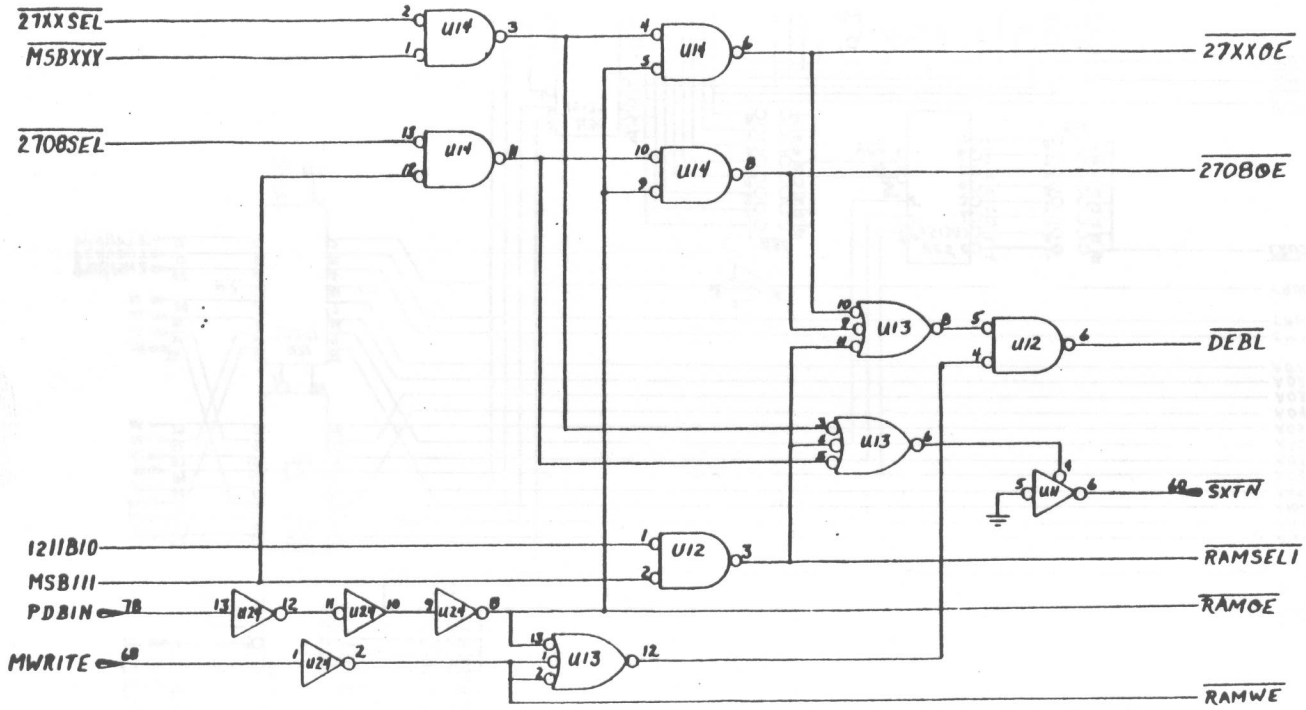
LTR	DESCRIPTION	DATE	APPROVED



CONTROL + SELECT LOGIC

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC.	ANGLES
±	±	±

APPROVALS	DATE
DRAWN	
CHECKED	

MARINCHIP SYSTEMS

PROM/RAM/SIO/RTC

SCALE	SIZE	DRAWING NO.
	B	

DO NOT SCALE DRAWING — SHEET 2

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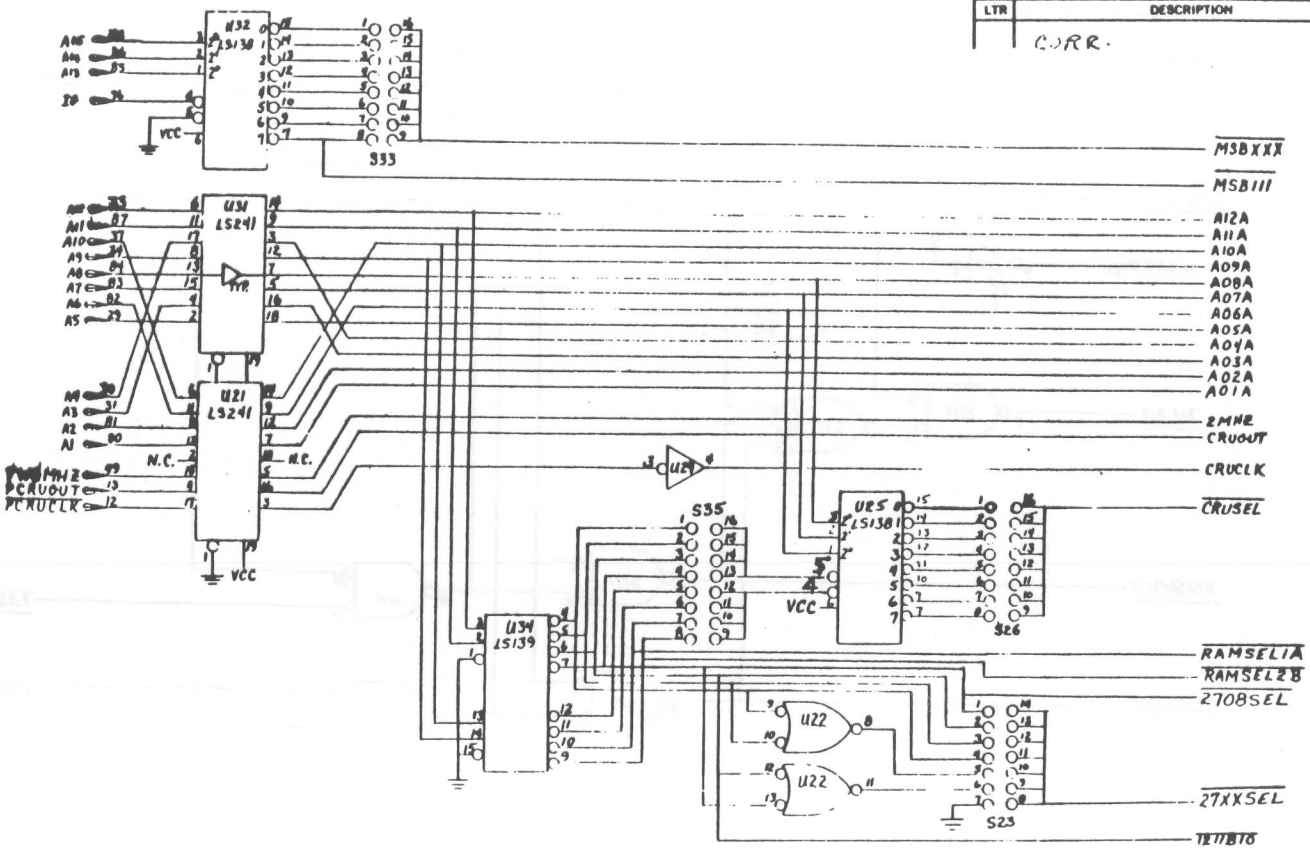
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
	CORR.	80 05 05	



BUS BUFFER + SELECTION

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC.	ANGLES
±	±	±

APPROVALS	DATE
DRAWN	
CHECKED	

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PROM/RAM/SIO/RTC

SCALE	SIZE	DRAWING NO.
	B	

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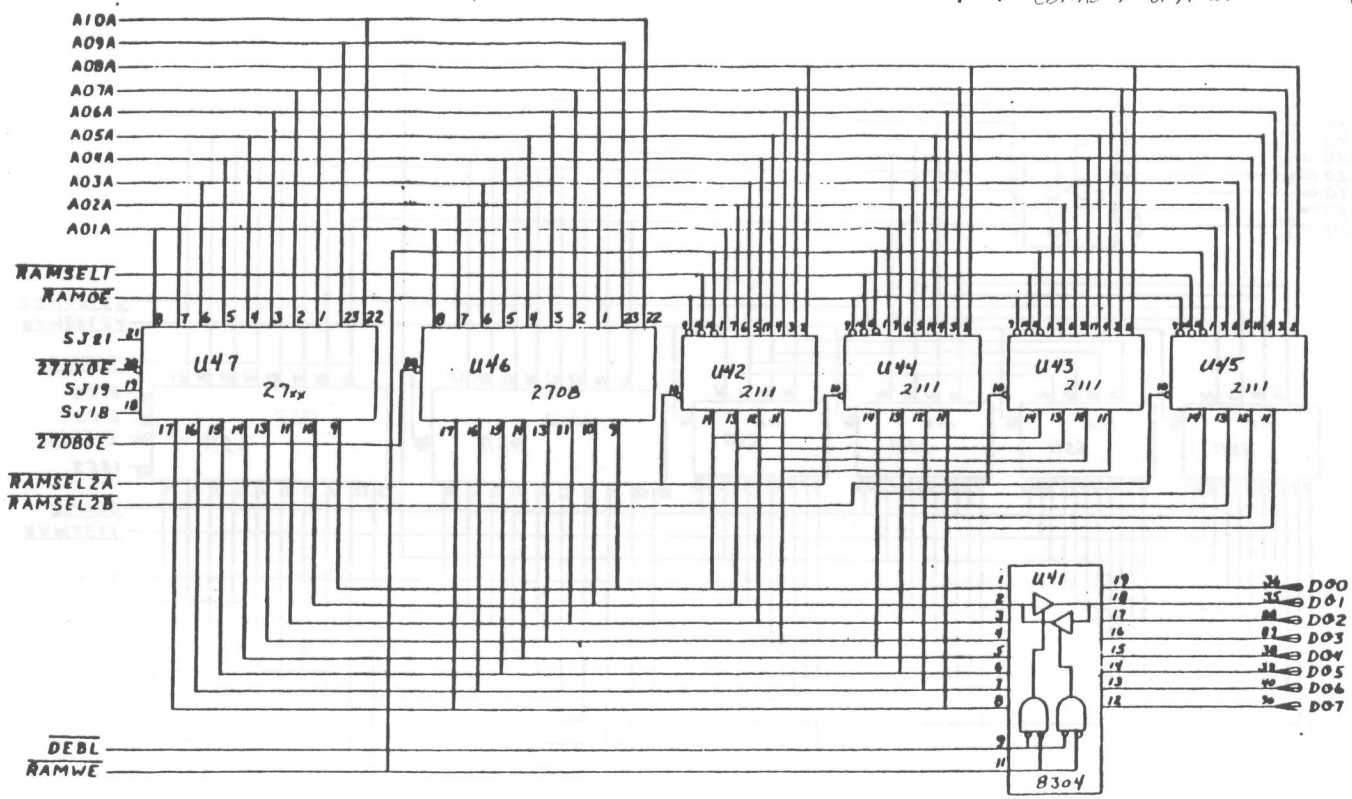
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
	CORRECT U41 NOTATION	790404	



EVEN ADDRESS MEMORY- DATA

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC. ANGLES ± ± ±		MARINCHIP SYSTEMS	
APPROVALS	DATE	PROM/RAM/SIO/RTC	
DRAWN			
CHECKED		SCALE	SIZE B / DRAWING NO.
		DO NOT SCALE DRAWING	SHEET 4

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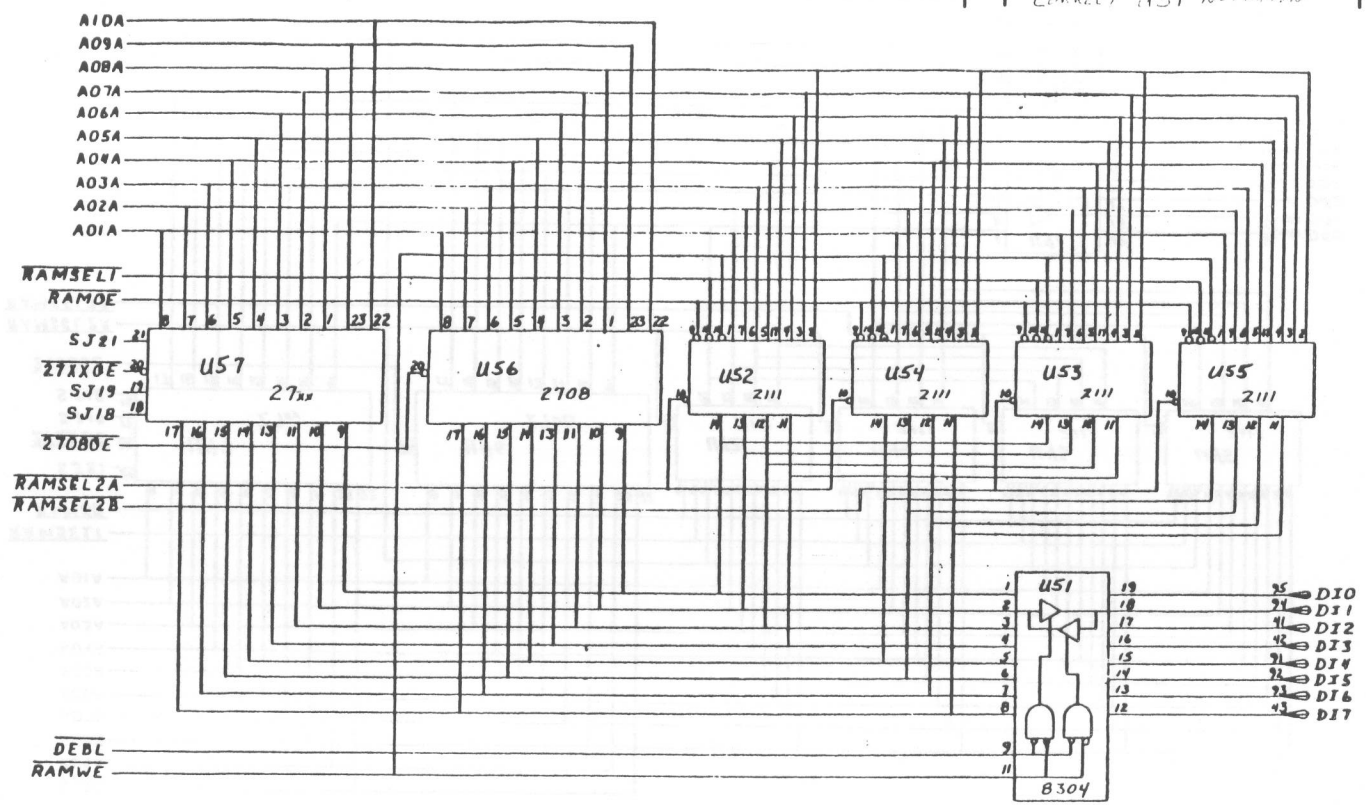
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
	CORRECT U51 NOTATION	790404	



ODD ADDRESS MEMORY - DATA

TOLERANCES UNLESS OTHERWISE SPECIFIED			
FRACTIONS ±	DEC. ±	ANGLES ±	
APPROVALS		DATE	
DRAWN			
CHECKED			

MARINCHIP SYSTEMS

PROM/RAM/SIO/RTC

SCALE	SIZE	DRAWING NO.
	B	

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